WHAT IS CLAIMED IS:

1. A microinstruction sequencer including a microinstruction sequencer stack comprising an array of memory cells and control logic, said microinstruction sequencer stack coupled to receive data and control values from one of a microinstruction sequencing logic and a microprocessor core unit.

2. The microinstruction sequencer of claim 1, wherein the microprocessor core unit is an execution unit.

3. The microinstruction sequencer of claim 1, wherein the microprocessor core unit is a retire unit.

4. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to:

generate a value of a microinstruction address;

add an intermediary value to the value of the microinstruction address to yield an incremented value;

send a control value to the microinstruction sequencer stack, said control value to cause the incremented value to be pushed onto the microinstruction sequencer stack; and

push the incremented value onto the microinstruction sequencer stack.

5. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to a microinstruction address multiplexer.

6. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to an immediate logic, said immediate logic to pass the value to the microinstruction core unit.

7. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to push a value in an immediate field of a microinstruction onto the microinstruction sequencer stack.

8. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to return to a reset state.

9. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to pop a value and send the popped value to an immediate logic.

10. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to send a value at the top of the microinstruction sequencer stack to an immediate logic.

11. A microinstruction sequencer including a microinstruction sequencer stack comprising an array of memory cells and control logic, said microinstruction sequencer stack coupled to receive data and control values from a microprocessor execution unit.

12. The microinstruction sequencer of claim 11, wherein the microprocessor execution unit includes logic to:

read a register value; and

communicate the register value to the microinstruction sequencer stack.

13. A microprocessor including a microinstruction sequencer comprising:

an array of memory cells dedicated to said microinstruction sequencer;

an address multiplexer coupled to said array of memory cells;

sequencing logic coupled to said address multiplexer and to said array of memory cells; and

a microprocessor core unit coupled to said array of memory cells.

14. The microinstruction sequencer of claim 13, wherein the microprocessor core unit is an execution unit.

15. The microinstruction sequencer of claim 13, wherein the microprocessor core unit is a retire unit.

16. A method of directing the sequence of execution of microinstructions during a call to and return from a subroutine, comprising:

receiving a microinstruction at a microinstruction sequencing logic;

pushing a value in a field of the microinstruction onto a microinstruction sequencer stack, the value is a return address of the subroutine;

executing the subroutine;

popping the value from the microinstruction sequencer stack to a microinstruction address multiplexer; and

returning to the return address of the subroutine by sequencing the value from the address multiplexer to a microinstruction sequencer.

17. The method of claim 16, wherein the value is the address of the call of the subroutine plus one.